MPU4 MEMORY MPU3
MEMORY , සි FEEDBACK FRAME MEMORY MPU2 MEMORY MEMORY ⋤ STATUS REGISTER OUTPUT IMAGE BUS 101 INPUT IMAGE BUS ADDRESS BUS FEEDBACK BUS Address Bus CONTROL PART 133/ DATA FLOW F | G. 1

APPROVED O.G. FIG.

BY CLASS SUBCLASS

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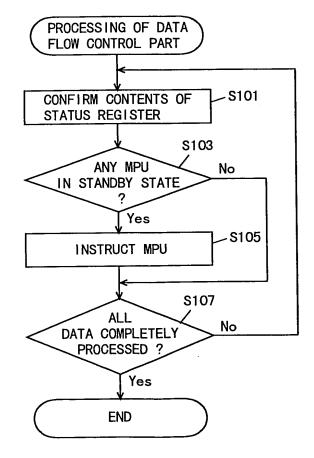
F I G. 2

EXEMPLARY STATUS REGISTER

	STANDBY	INPUT	PROCESSING	END OF PROCESSING	OUTPUT
MPU1	0	1	0	0	0
MPU2	1	0	0	0	0
MPU3	0	0	1	0	0
MPU4	0	0	О	0	1

FIG. 3

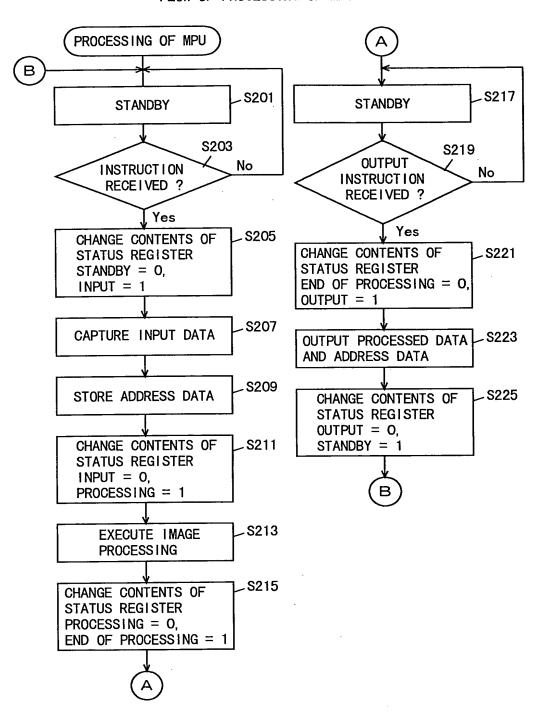
FLOW OF PROCESSING OF DATA FLOW CONTROL PART



APPROVED	O.G. FIG.		
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F I G. 4

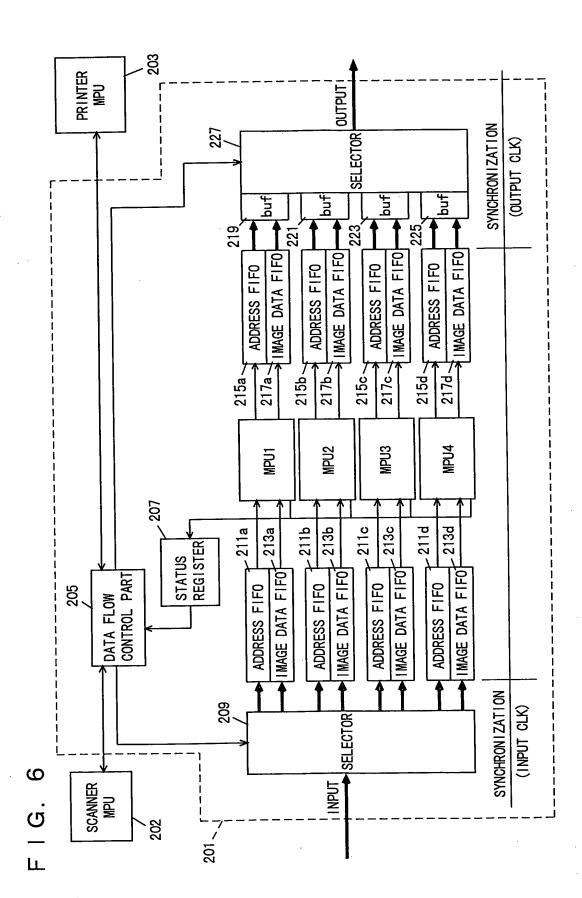
FLOW OF PROCESSING OF MPU

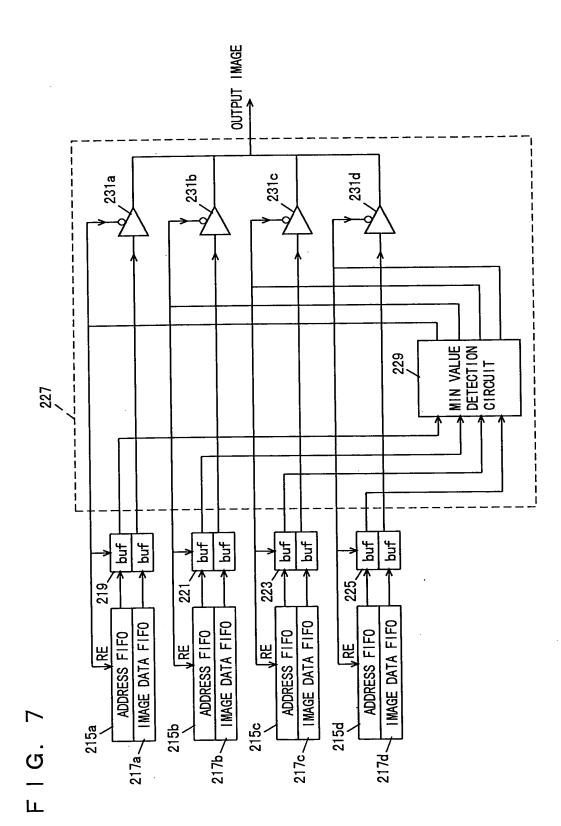


L

R3 쯆 A23 A20 A21 023 020 021 **B3** A30 සු **B31 D23 D21** D30 D 20 ន្ធ **K**2 器 A12 A13 A10 013 020 021 022 023 **D22** 011 002 A11 A02 012 010 11 010 011 012 OUTPUT DATA | Q01 | Q03 | Q00 ADDRESS DATA | A01 A03 A00 D02 8 8 \sqsubseteq 器 MPU2 MPU4 <u>P</u> MPU3 200 INPUT DATA 100 001 Ŋ н С

Dougher, 111299





F I G. 8

OPERATION OF SELECTOR 227

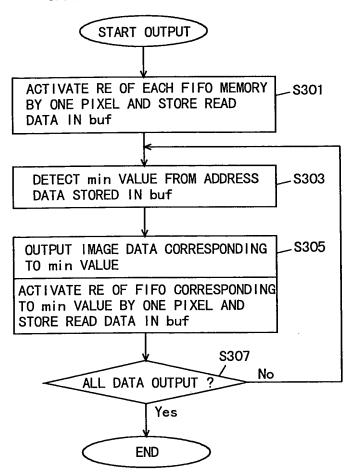


FIG. 9

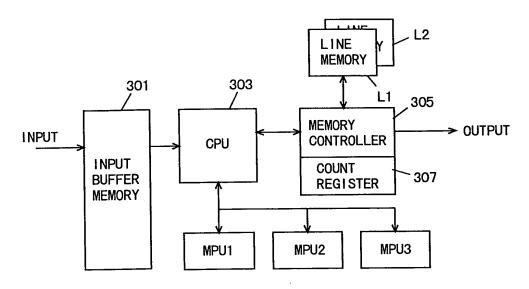
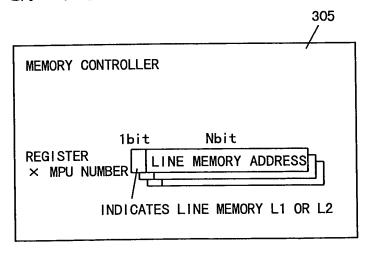


FIG. 10



APPROVED

FIG. 11

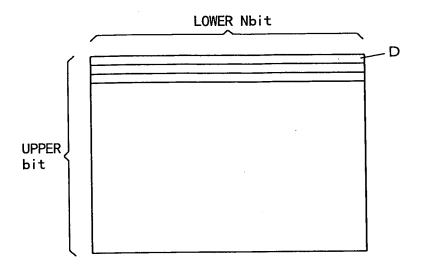


FIG. 12

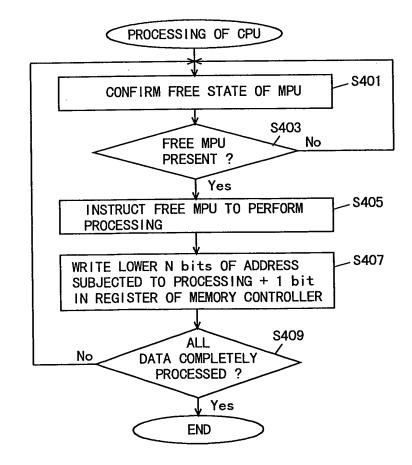


FIG. 13

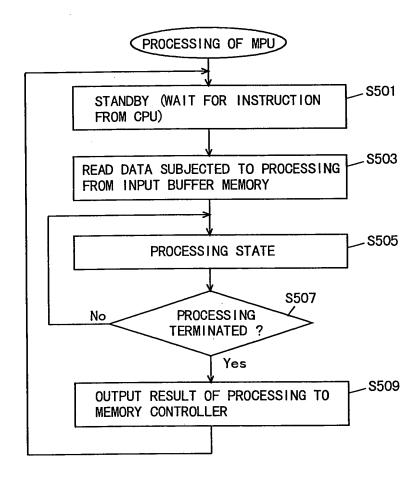


FIG. 14

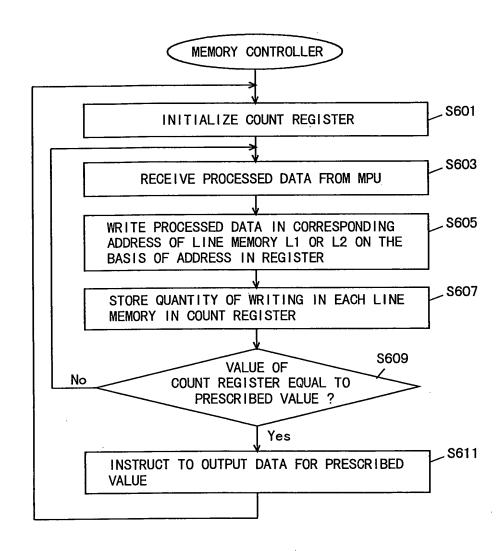


FIG. 15

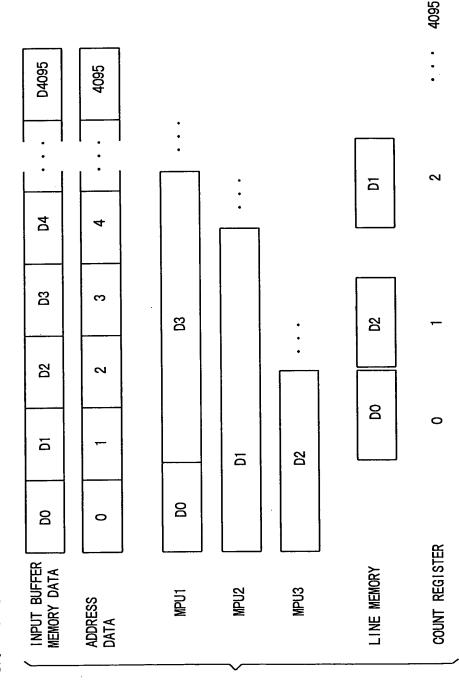


FIG. 16

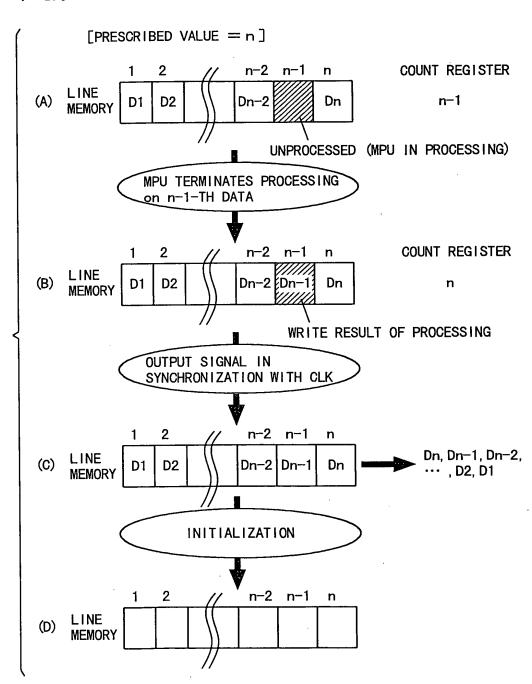


FIG. 17

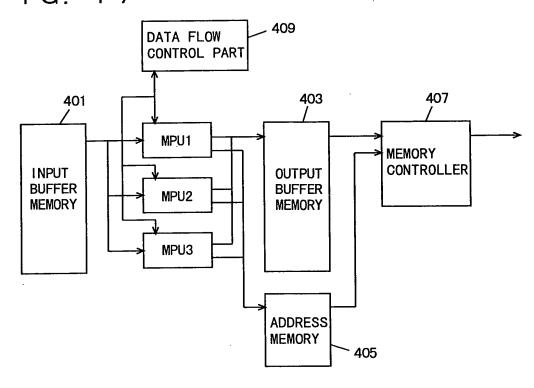
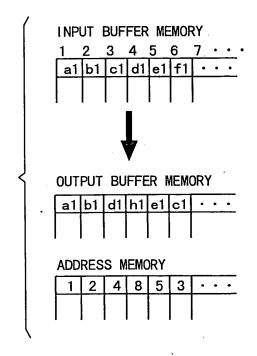
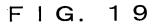
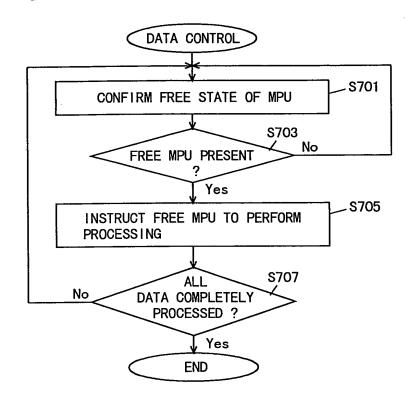


FIG. 18





[DATA FLOW CONTROL PART]



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FIG. 20

[FLOW OF PROCESSING OF MPU]

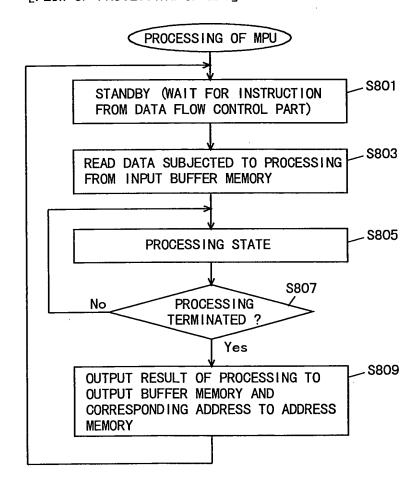
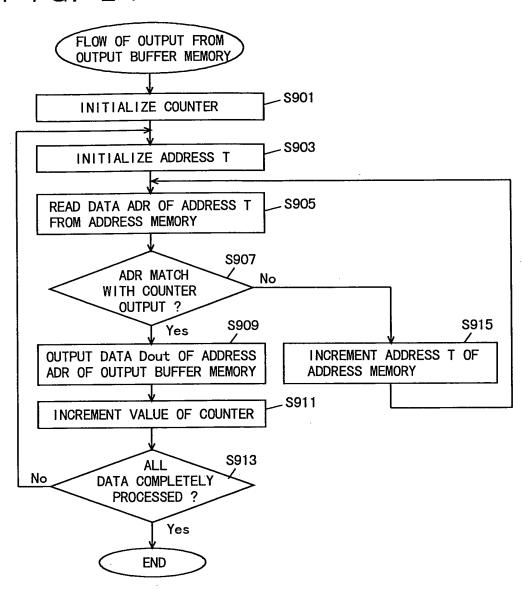


FIG. 21



APPROVED O.G. FIG.
BY CLASS SUBCLASS
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FIG. 22

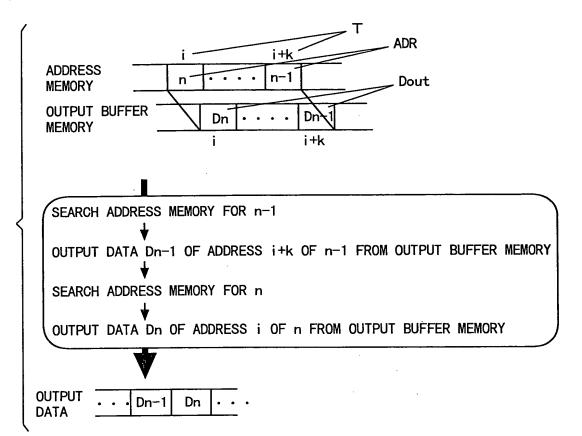
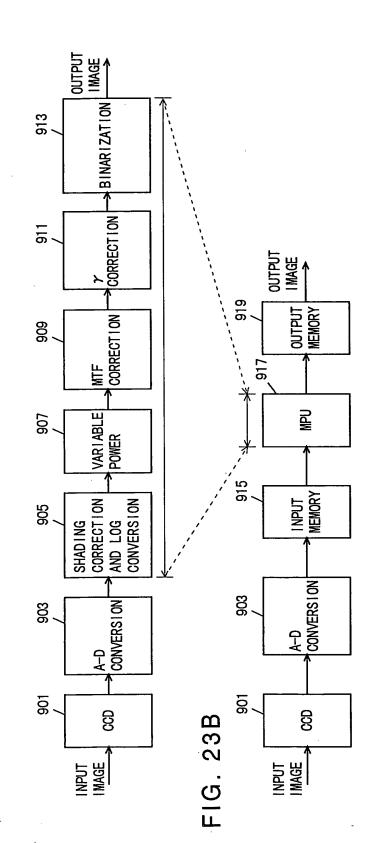


FIG. 25

L1 ↓	L2 	L3 	L4 ↓
D00	D01	D02	D03
D10	D11	D12	D13
D20	D21	D22	D23
D30	D31	D32	D33
D40	D41	D42	D43
D50	D51	D52	D53

FIG. 23A



APPROVED	O.G. FIG.		
BY	CLASS	SUBCLASS	
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MPU4 MPU3 , 951 FEEDBACK FRAME MEMORY MPU₂ MPU1 952 STATUS | REGISTER OUTPUT IMAGE BUS INPUT IMAGE BUS DATA FLOW CONTROL PART FEEDBACK BUS 953 7

F I G. 24



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